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EXAMINER	
GEIB, BENJAMIN P	

ART UNIT	PAPER NUMBER
2181	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/815,478	BALL, JAMES LORAN	
	Examiner	Art Unit	
	BENJAMIN P. GEIB	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 November 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8,14-19,31 and 32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8,14-19,31 and 32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *11/06/2008*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 31 and 32 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

3. Claims 31 and 32 recite limitations referring to “the array.” However, there is no previous mention within the claims of an “array," and, therefore, the limitations render the claims indefinite. Because the intent of the limitations of claims 31 and 32 is unclear and any interpretation by the examiner would be a mere guess, claims 31 and 32 will be interpreted as not further limiting the invention.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-8 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Intel, Inc. (I—32® Architecture Software Developer’s Manual, Volumes 1-2, 2002), hereinafter Intel, in view of Killian et al. (U.S. Patent No. 5,420,992), hereinafter Killian.

6. Regarding claim 1, Intel teaches a processor, comprising:

a plurality of registers *[see Intel, Vol. 1, Page 3-8, section 3.4]*;

circuitry configured to process a plurality of instructions *[see Intel, Vol. 1, Page 2-14, Section 2.6.2]* associated with an instruction set including a plurality of branch and non-branch instructions *[see Intel, Vol. 2, section 3.2, starting on page 3-15; Examiner's note: section 3.2 provides a listing of all*

instruction able to be processed by the P6 architecture, including branch (i.e., JMP, Jcc, CALL, et al.) and non-branch instructions (i.e., ADD, AND, CMP, et al.).], the plurality of instructions each having a multi-byte length *[see Intel, Vol. 2, page 2-1, section 2.1]*, the plurality of instructions accessible at multi-byte aligned addresses *[see Intel, Vol. 1, Page 1-7, Fig. 1-1; Examiner's note: Since the IA-32 architecture employs 32-bit instructions, these instructions would be accessed by multi-byte aligned addresses.]*;

wherein substantially all multi-byte aligned branch instructions are operable to access the instructions at byte aligned addresses *[see Intel, Vol. 2, page 3-357 "JMP-Jump" instruction reference; page 3-358, line 1-2, "A relative offset (rel8, rel16, or rel32) is generally specified as a label in assembly code, but at the machine code level, it is encoded as a signed 8-, 16-, or 32-bit immediate value."; Examiner's note: In the description of operating modes, Intel discloses a jump instruction that uses an offset corresponding to 8 bits (JMP rel8) as well as other indexing modes (rel16, rel32 et al.)]* .

Intel does not teach common subcircuitry operable perform sign extensions of an immediate field in non-branch instructions and to perform sign extensions of said immediate field in branch instructions to calculate a target address for branch instructions, wherein said common subcircuitry operating on said non-branch instructions is the same subcircuitry operating upon said branch instructions.

Killian teaches common subcircuitry operable to perform sign extensions of an immediate field in non-branch instructions and to perform sign extensions of said immediate fields in branch instructions to calculate a target address for branch instructions, wherein said common subcircuitry operating on said non-branch instructions is the same subcircuitry operating upon said branch instructions (See column 8, lines 7-13, Figure 3C).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to have modified Intel to include the common subcircuitry operable to perform sign extensions of an immediate field in non-branch instructions and to perform sign extensions of said immediate field in branch instructions to calculate a target address for branch instructions, wherein said common subcircuitry operating on said non-branch instructions is the same subcircuitry operating upon said branch instructions, as taught by Kiillian. Intel already teaches the necessity of sign extending branch immediates (See Intel, Vol. 2,page 3-358, line 1-2: "A relative offset (rel8, rel16, or rel32) is generally

specified as a label in assembly code, but at the machine code level, it is encoded as a signed 8-, 16-, or 32-bit immediate value."). Sign extensions of immediates are done for various types of operations within the ALU in the Intel architecture. One having ordinary skill in the art would recognize that having a common subcircuitry perform both sign extensions of branches and non-branches would increase the overall functionality and efficiency of the system.

7. Regarding claim 2, Intel and Killian have taught the processor of claim 1, wherein the plurality of instructions are accessed at word aligned addresses *[see Intel, Vol. 2, Page 3-358, line 1-2, "…it is encoded as a signed 8-, 16-, or 32-bit immediate value."; Examiner's note: Intel discloses a 32-bit offset, thus word aligned addresses.]*.

8. Regarding claim 3, Intel and Killian have taught a processor of claim 1, wherein the plurality of instructions are accessed at half-word aligned addresses *[see Intel, Vol. 2, Page 3-358, line 1-2, "…it is encoded as a signed 8-, 16-, or 32-bit immediate value."; Examiner's note: Intel discloses a 16-bit offset, thus half-word aligned addresses.]*.

9. Regarding claim 4, Intel and Killian have taught the processor of claim 1, wherein accessing the instructions comprises reading and writing the addresses *[see Intel, Vol. 2, Page 3-357; lines 1-7, "Transfers program control to…a memory location"; Vol. 2, Page 3-359, Operation Code, line 4, "tempEIP <- EIP + DEST"; Examiner's note: In the operation of the jump instruction, Intel discloses reading the address (offset or absolute) from the instruction, as illustrated by "DEST", and writing the address to "tempEIP" for use in changing the instruction pointer.]*.

10. Regarding claim 5, Intel and Killian have taught the processor of claim 1, wherein branch instructions comprise branch and conditional branch instructions *[see Intel, Vol. 2, section 3.2, instructions (sections) Jcc (conditional jump) and JMP (jump)]*.

11. Regarding claim 6, Intel and Killian have taught the processor of claim 1, wherein branch instructions comprise a branch offset and a current program counter value *[see Intel, Vol. 2, Page 3-359, Operation Code, line 4, "tempEIP <- EIP + DEST"; Examiner's note: In this cite, Intel discloses an offset (DEST) being added to the program counter value (EIP).]*.

12. Regarding claim 7, Intel and Killian have taught the processor of claim 1, wherein the units of the branch offset *[see Intel, Vol. 2, Page 3-357, "JMP rel8", "When executing a near jump the processor jumps to the address…that is specified with the target operand"]* and the current program counter are in bytes *[see Intel, Vol. 1, Page 3-8, section 3.4, lines 9-10, "EIP (instruction pointer) register…contains a 32-bit pointer…"; Examiner's note: A 32-bit value is comprised of four 8-bit bytes.]*.

13. Regarding claim 8, Intel and Killian have taught the processor of claim 1, wherein the plurality of instructions are one word in length *[see Intel, Vol. 1, Page 1-7, Fig. 1-1; Examiner's note: It would have been well known that the IA-32 architecture utilizes 32-bit instructions.]*.

14. Referring to claim 31, Intel and Killian have taught the processor of claim 1, wherein one of a primary or secondary component accesses memory of the array directly through ports without access through a system bus, and wherein the array does not comprise a system bus.

15. Claims 14-19 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Intel in view of Killian, and further in view of Wittig et al., "OneChip: An FPGA Processor with Reconfigurable Logic" (hereinafter Wittig).

16. Regarding claim 14, Intel teaches a processor, comprising:

a plurality of registers *[see Intel, Vol. 1, Page 3-8, section 3.4]*;

circuitry *[see Intel, Vol. 1, Page 2-14, Section 2.6.2]* configured to process a plurality of branch and non-branch instructions associated with an instruction set *[see Intel, Vol. 2, section 3.2, starting on page 3-15; Examiner's note: section 3.2 provides a listing of all instruction able to be processed by the P6 architecture, including branch (i.e., JMP, Jcc, CALL, et al.) and non-branch instructions (i.e., ADD, AND, CMP, et al.).]*, the plurality of branch instructions and non-branch instructions including an immediate field *[see Intel, Vol. 2, Page 3-21, line "Add imm8 to AL"; Page 3-357, lines 3-4 "This operand can be an immediate value, a general-purpose register, or a memory location."]*; wherein common subcircuitry *[see Intel, Vol. 1, Page 2-10, Figure 2-1, element "Execution Out-of-Order Core"; Vol. 1, Page 2-14, section 2.6.2;]* is used to process the immediate field associated with one or more branch instructions and one or

more non-branch instructions *[see Intel, Vol. 2, page 3-21, lines 2-3 "The destination operand can be a register or a memory location; the source operand can be an immediate, a register, or a memory location." (use of immediate processing with non-branch (ADD) instructions); Page 3-357, lines 3-4 "This operand can be an immediate value, a general-purpose register, or a memory location." (use of immediate processing with branch instructions). Examiner's note: It is clear from the Intel disclosure and would have been well known at the time of invention that the P6 processor employs sub circuitry (the execution core) to perform multiple operations, including branch and non-branch instructions. Furthermore, since the IA-32 architecture utilizes immediate fields in both branch and non-branch (i.e., adding an immediate value) instructions, said instructions would both be executed by said sub circuitry, such as an adder to compute the addition or target address, as was common knowledge at the time of invention.].*

Intel does not teach wherein said common subcircuitry operating on said non-branch instructions is the same subcircuitry operating upon said branch instructions, wherein the circuitry is operable perform sign extensions of immediate fields in non-branch instructions and perform sign extensions of immediate fields in branch instructions to calculate a target address for branch instructions.

Killian teaches a common subcircuitry operating on said non-branch instructions is the same subcircuitry operating upon said branch instructionsm wherein the common subcircuitry is configured to perform sign extensions of immediate fields in non-branch instructions and perform sign extensions of immediate fields in branch instructions to calculate a target address for branch instructions (See column 8, lines 7-13, Figure 3C).

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to have modified Intel to include a common subcircuitry that is configured to perform sign extensions of immediate fields in non-branch instructions and perform sign extensions of immediate fields in branch instructions to calculate a target address for branch instructions, and wherein said common subcircuitry operating on said non-branch instructions is the same subcircuitry operating upon said branch instructions, as taught by Killian. Intel already teaches the necessity of sign extending branch immediates (See Intel, Vol. 2,page 3-358, line 1-2: "A relative offset (rel8, rel16, or rel32) is generally

specified as a label in assembly code, but at the machine code level, it is encoded as a signed 8-, 16-, or 32-bit immediate value."). Sign extensions of immediates are done for various types of operations within the ALU in the Intel architecture. One having ordinary skill in the art would recognize that having a common subcircuitry perform sign extensions of branches and non-branches would increase the overall functionality and efficiency of the system.

Intel and Killian have not taught that the processor is in a field programmable gate array.

Wittig has taught incorporating a processor within a field programmable gate array *[See Wittig, Introduction]*.

At the time the invention was made, it would have been obvious to one of ordinary skill in the art to incorporated the processor of Intel and Killian within a field programmable gate array.

The motivation for doing so would be to allow closely coupled access to programmable logic, thereby improving performance of applications requiring the programmable logic *[See Wittig, Introduction]*.

17. Regarding claim 15, Intel, Killian, and Wittig have taught the field programmable gate array of claim 14, wherein the instruction set comprises a plurality of instructions *[see Intel, Vol. 2, section 3.2 (listing of a plurality of instructions supported by the P6 architecture.]*.

18. Regarding claim 16, Intel and Killian have taught the field programmable gate array of claim 15, wherein the plurality of instructions are accessed at half-word aligned addresses *[see Intel, Vol. 2, Page 3-358, line 1-2, "…it is encoded as a signed 8-, 16-, or 32-bit immediate value"; Examiner's note: Intel discloses a 16-bit offset, thus half-word aligned addresses.]*.

19. Regarding claim 17, Intel, Killian, and Wittig have taught the field programmable gate array of claim 14, wherein branch instructions comprise branch and conditional branch instructions *[see Intel, Vol. 2, section 3.2, instructions (sections) Jcc (conditional jump) and JMP (jump)]*.

20. Regarding claim 18, Intel, Killian, and Wittig have taught the field programmable gate array of claim 14, wherein common subcircuitry *[see Intel, Vol. 1, Page 2-10, Figure 2-1, element "Execution Out-of-Order Core"; Vol. 1, Page 2-14, section 2.6.2;]* is used to handle the immediate field associated with the branch and non-branch instructions and wherein an immediate field value is maintained in units of

bytes *[see Intel, Vol. 2, page 3-21, lines 2-3 "The destination operand can be a register or a memory location; the source operand can be an immediate, a register, or a memory location." (use of immediate processing with non-branch (ADD) instructions); Page 3-357, lines 3-4 "This operand can be an immediate value, a general-purpose register, or a memory location." (use of immediate processing with branch instructions). Examiner's note: It is clear from the Intel disclosure and would have been well known at the time of invention that the P6 processor employs sub circuitry (the execution core) to perform multiple operations, including branch and non-branch instructions. Furthermore, since the IA-32 architecture utilizes immediate fields in both branch and non-branch (i.e., adding an immediate value) instructions, said instructions would both be executed by said sub circuitry, such as an adder to compute the addition or target address, as was common knowledge at the time of invention.].*

21. Regarding claim 19, Intel, Killian, and Wittig have taught the field programmable gate array of claim 18, wherein common subcircuitry is used to perform sign-extensions of the immediate field associated with the branch and non-branch instructions *[see Intel, Vol. 2, Page 3-3, point 4, "imm8—An immediate byte value. The imm8 symbol is a signed number between –128 and +127 inclusive. For instructions in which imm8 is combined with a word or doubleword operand, the immediate value is sign-extended to form a word or doubleword. The upper byte of the word is filled with the topmost bit of the immediate value." Examiner's note: As cited multiple time in this action, many instructions (branch and non-branch) utilize an immediate byte value thus would be sign extended by the execution core.].*

22. Referring to claim 32, Intel, Killian, and Wittig have taught the field programmable gate array of claim 14, wherein one of a primary or secondary component accesses memory of the array directly through ports without access through a system bus, and wherein the array does not comprise a system bus.

Response to Arguments

23. Applicant's arguments filed 11/06/2008 have been fully considered but they are not persuasive.

24. The applicant argues the novelty/rejection of the claims, in substance that:

a) “Intel, alone or in combination with Killian, fails to teach or render obvious the claim 1 limitation of ‘common subcircuitry operable to perform sign extensions of an immediate field in non-branch instructions and to perform sign extensions of said immediate field in branch instructions to calculate a target address for branch instructions, wherein said common subcircuitry operating on said non-branch instructions is the same subcircuitry operation upon said branch instructions.’” (4th paragraph on page 6)

b) “Intel, alone or in combination with Killian and Solomon, fails to teach such a field programmable gate array (“FPGA”). (last paragraph on page 7)

c) “Intel, alone or in combination with Killian and Solomon fails to teach the amended limitation 'wherein common subcircuitry is used to handle the immediate field associated with the branch and non-branch instructions and wherein an immediate field value is maintained in units of bytes.’” (2nd paragraph on page 8)

25. These arguments are not found persuasive for the following reasons:

Regarding point a, it appears to the examiner that the applicant is arguing against the references individually. One cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). As described in the rejection of claim 1, while neither Intel nor Killian separately teach the entirety of claim 1, the combination of the two references render the claim obvious. Regarding the obviousness of claim 1, the applicant merely states that the claim indicates "a non-obvious and non-trivial improvement" and cites to an area of the specification describing the claimed invention without particularly pointing out why the combination would be non-obvious.

Regarding point b, the applicant's arguments have been considered but are moot in view of the new grounds of rejection.

Regarding point c, Intel has taught that the memory is byte addressable (See Intel, page 3-3). Therefore, any address value, including an immediate field value, is maintained in units of bytes.

Conclusion

26. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date

of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to BENJAMIN P. GEIB whose telephone number is (571)272-8628. The examiner can normally be reached on Mon-Fri 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alford Kindred can be reached on (571) 272-4037. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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